

Control integrated Power System (CIPOS™)

IKCS17F60B2A

IKCS17F60B2C

<http://www.infineon.com/cipos>

Power Management & Drives



N e v e r s t o p t h i n k i n g .

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Page	Subjects (major changes since last revision)
4	Added UL certification
10	Change $V_{IT,HYS}$

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Internal Electrical Schematic

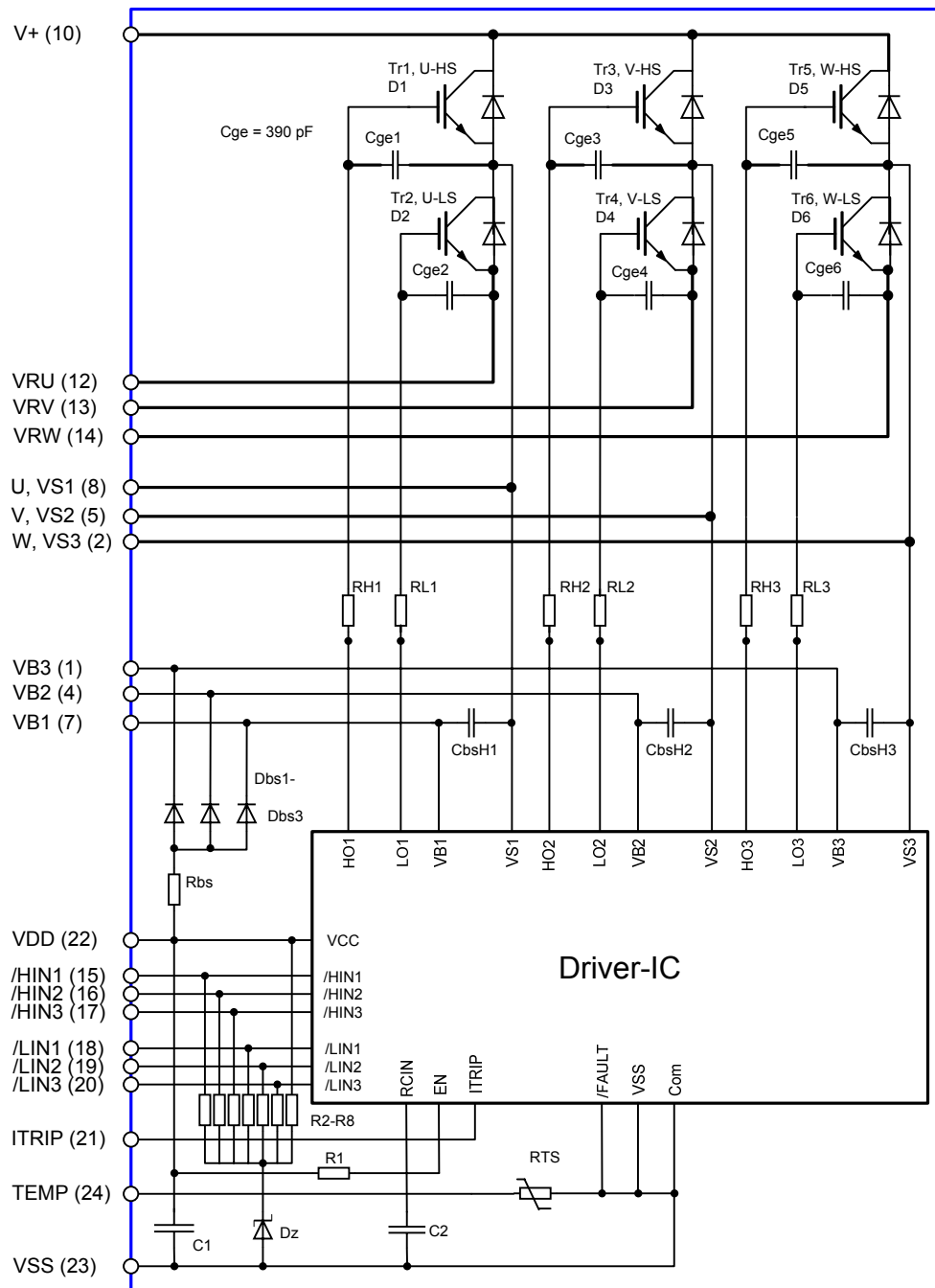


Figure 1: Internal Schematic

Pin Assignment

Pin Number	Pin Name	Pin Description
1	VB3	high side floating IC supply voltage
2	W,VS3	motor output W, high side floating IC supply offset voltage
3	n.a.	None
4	VB2	high side floating IC supply voltage
5	V,VS2	motor output V, high side floating IC supply offset voltage
6	n.a.	None
7	VB1	high side floating IC supply voltage
8	U,VS1	motor output U, high side floating IC supply offset voltage
9	n.a.	None
10	V+	positive bus input voltage
11	n.a.	None
12	VRU	low side emitter
13	VRV	low side emitter
14	VRW	low side emitter
15	/HIN1	input gate driver high side 1/U
16	/HIN2	input gate driver high side 2/V
17	/HIN3	input gate driver high side 3/W
18	/LIN1	input gate driver low side 1/U
19	/LIN2	input gate driver low side 2/V
20	/LIN3	input gate driver low side 3/W
21	ITRIP	input overcurrent shutdown
22	VDD	module control supply
23	VSS	module negative supply
24	TEMP	temperature monitoring

Pin Description

/HIN1,2,3 and /LIN1,2,3 (Low side and high side control pins, Pin 15 - 20)

These pins are active low and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility.

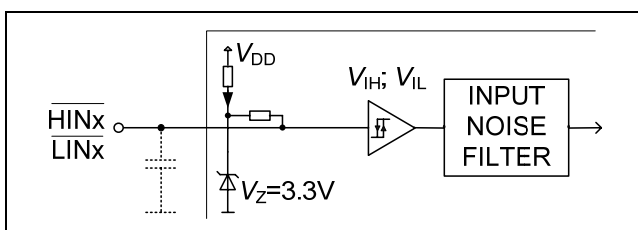


Figure 2: Input pin structure

down to 3.3V controller outputs. The maximum voltage at these pins is 5.5V and therefore fully compliant to 3.3V-microcontrollers. Pull-up resistor of about 75 kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

It is recommended for proper work of CIPOS™ not to provide an input pulse-width and PWM deadtimes lower than 1μs.

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3).

A minimum deadtime insertion of typ 380ns is also provided, in order to reduce cross-conduction of the external power switches.

TEMP (temperature NTC, Pin 24)

The TEMP terminal provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5V ensures, that the resulting voltage can be directly connected to the microcontroller.

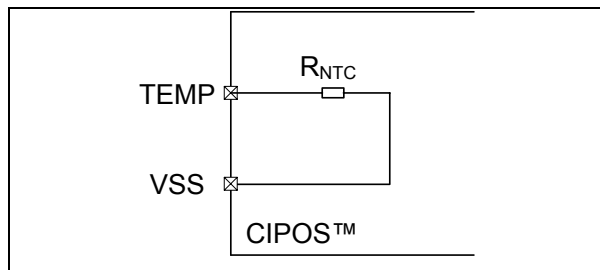


Figure 3: Internal Circuit at pin TEMP

ITRIP (Over-current detection function, Pin 21)

CIPOS™ provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.46V) is referenced to VSS ground. A input noise filter (typ: $t_{ITRIPMIN} = 220ns$) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver after the shutdown propagation delay of typically 1000ns.

The fault-clear time is set to typically to 4.7ms.

VDD, VSS (control side supply and reference, Pin 22, 23)

VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 12.1 V$ is at least present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below $V_{DDUV-} = 10.4 V$. This prevents the external power

switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB1,2,3 and VS1,2,3 (High side supplies, Pin 1, 2, 4, 5, 7, 8)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage.

Due to the low power consumption, the floating driver stage is supplied by an integrated bootstrap circuit connected to VDD. This includes also integrated bootstrap capacitors of 100 nF at each floating supply, which are located very close to the gate drive circuit.

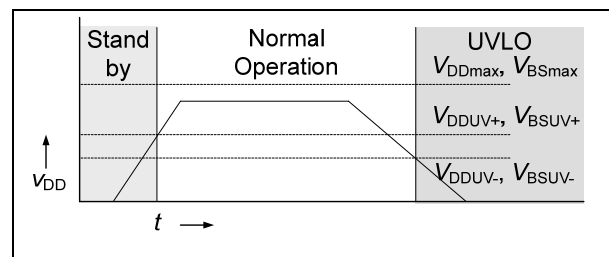


Figure 4: Input filter timing diagram

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 12.1 V$ and a falling threshold of $V_{DDUV-} = 10.4 V$ according to Figure 4.

VS1,2,3 provide a high robustness against negative voltage in respect of VSS of -50 V. This ensures very stable designs even under rough conditions.

VRU, VRV, VRW (low side emitter, Pin 12, 13, 14)

The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

V+ (positive bus input voltage, Pin 10)

The high side IGBT are connected to the bus voltage. It is recommended, that the bus voltage does not exceed 500 V.

Absolute Maximum Ratings

($T_c = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$, if not stated otherwise)

Module Section

Description	Condition	Symbol	Value		Unit
			Min	max	
Storage temperature range		T_{stg}	-40	125	$^\circ\text{C}$
Operating temperature control PCB ¹		T_{PCB}	-	125	$^\circ\text{C}$
Solder temperature	Wave soldering, 1.6mm (0.063in.) from case for 10s	T_{sol}	-	260	$^\circ\text{C}$
Insulation test voltage	RMS, $f=50\text{Hz}$, $t=1\text{min}$	V_{ISOL}	2500	-	V
Mounting torque	M3 screw and washer	M_S	-	0.6	Nm
Mounting pressure on surface	Package flat on mounting surface	N_{MC}	-	150	N/mm ²
Creepage distance		d_S	3.1	-	mm
Max. peak power of bootstrap resistor	$t_p = 100\mu\text{s}$ $T_c = 100^\circ\text{C}$	P_{BRpeak}		90	W

IGBT and Diode Section

Description	Condition	Symbol	Value		Unit
			min	max	
Max. Blocking Voltage		V_{CES}	600	-	V
DC output current	$T_c = 25^\circ\text{C}, T_{\text{vj}} < 150^\circ\text{C}$ $T_c = 80^\circ\text{C}, T_{\text{vj}} < 150^\circ\text{C}$	I_u, I_v, I_w	-17 -10	17 10	A
Repetitive peak collector current	t_p limited by T_{vjmax}	I_u, I_v, I_w	-30	30	A
Short circuit withstand time ²	$V_{DD} = 15\text{V}, V_{DC} = 400\text{V}$, $T_{\text{vj}} = 150^\circ\text{C}$	t_{sc}	-	5	μs
IGBT reverse bias safe operating area (RBSOA)	$V_{DD} = 15\text{V}, V_{DC} \leq 500\text{V}$, $T_{\text{vj}} = 150^\circ\text{C}, I_c = 10\text{A}$ $V_{\text{CEmax}} = 600\text{V}$		Full Square		
Power dissipation per IGBT	$T_c = 25^\circ\text{C}$	P_{tot}	-	52	W
Operating junction temperature range	IGBT Diode	T_{vjI} T_{vjD}	-40 -40	150 150	$^\circ\text{C}$

¹ Monitored by pin 24

² Allowed number of short circuits: <1000; time between short circuits: >1s.

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Single IGBT thermal resistance, junction-case		R_{thJC}	-	-	2.4	K/W
Single diode thermal resistance, junction-case		R_{thJCD}	-	-	3.6	

Control Section

Description	Condition	Symbol	Value		Unit
			min	max	
Module supply voltage		V_{DD}	-1	20	V
High side floating supply voltage (V_B vs. V_S)		V_{BS}	-1	20	
High side floating IC supply offset voltage	$t_p < 500ns$	$V_{S1,2,3}$	$V_{DD}-V_{BS}-6$ $V_{DD}-V_{BS}-50$	600	
ITRIP Input voltage		$V_{IN,ITRIP}$	-1	10	
/HIN, /LIN Input voltage	$V_{IN} = \text{float}$	V_{IN}	-1	5.5	
Operating junction temperature ¹		$T_{J,IC}$	-	125	°C
Max. switching frequency		f_{PWM}	-	20	kHz

Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -Potential unless otherwise specified.

Description	Symbol	Value		Unit
		min	max	
High side floating supply offset voltage	V_S	-3	500	V
High side floating supply voltage (V_B vs. V_S)	V_{BS}	12.5	17.5	
Low side power supply	V_{DD}	12.5	17.5	
Logic input voltages LIN, HIN, ITRIP	V_{IN}	0	5	

¹ Monitored by pin 24

Static Characteristics

($T_c = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Collector-Emitter breakdown voltage	$V_{IN} = 5\text{V}$, $I_C = 0.25\text{mA}$	$V_{(BR)CES}$	600			V
Collector-Emitter saturation voltage	$V_{DD} = 15\text{V}$, $I_{out} = \pm 10\text{A}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	$V_{CE(sat)}$	-	1.65	2.1	V
			-	1.9		
Diode forward voltage	$V_{IN} = 5\text{V}$, $I_{out} = \pm 10\text{A}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	V_F	-	1.7	2.05	V
			-	1.6		
Zero gate voltage collector current of IGBT	$V_{CE} = 600\text{V}$, $V_{DD} = 5\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	I_{CES}	-	-	40	μA
			-	-	1000	
Short circuit collector current ¹	$V_{DD} = 15\text{V}$, $t_{SC} \leq 5\mu\text{s}$ $V_{CC} = 300\text{V}$, $T_j = 150^\circ\text{C}$	$I_{C(SC)}^2$	-	65	-	A
Logic "0" input voltage (LIN,HIN)		V_{IH}	1.7	2.1	2.4	V
Logic "1" input voltage (LIN,HIN)		V_{IL}	0.7	0.9	1.1	V
ITRIP positive going threshold		$V_{IT,TH+}$	360	460	540	mV
ITRIP input hysteresis		$V_{IT,HYS}$	45	75	-	mV
V_{DD} and V_{BS} supply undervoltage positive going threshold		V_{DDUV+}^2 V_{BSUV+}^2	11.0	12.1	12.8	V
V_{DD} and V_{BS} supply undervoltage negative going threshold		V_{DDUV-}^2 V_{BSUV-}^2	9.5	10.4	11.0	V
V_{CC} and V_{BS} supply undervoltage lockout hysteresis		V_{DDUVH}^2 V_{BSUVH}^2	1.2	1.7	-	V
Input clamp voltage (/HIN, /LIN)	$I_{IN} = 4\text{mA}$	$V_{INCLAMP}$	-	10.4	13	V
Input clamp voltage (ITRIP)	$I_{IN} = 4\text{mA}$	$V_{INCLAMP}$	-	10.6	13	V
Quiescent V_{Bx} supply current (V_{Bx} only)	$V_{HIN} = \text{low}$	I_{QB}	-	300	550	μA
Quiescent V_{DD} supply current (V_{DD} only)	$V_{IN} = \text{float}$	I_{QDD}	-	2.4	3.4	mA
Input bias current	$V_{IN} = 5\text{V}$	I_{IN+}	-	55	100	μA
Input bias current	$V_{IN} = 0\text{V}$	I_{IN-}	-	220	400	μA
ITRIP Input bias current	$V_{ITRIP} = 5\text{V}$	I_{ITRIP+}	-	75	120	μA
Leakage current of high side	$T_{j,IC} = 125^\circ\text{C}$	I_{LVS}^2	-	30	-	μA
FAULT low on resistance of the pull down transistors	$V_{FLT} = 0.5\text{V}$, $V_{ITRIP} = 1\text{V}$	$R_{on,FLT}$	-	56	-	Ω

¹ Allowed number of short circuits: <1000; time between short circuits: >1s.

² Test is not subject of product test, verified by characterisation

Dynamic Characteristics

($T_c = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$, if not stated otherwise)

Description	Condition	Symbol	Value			Unit
			min	typ	max	
Turn-on propagation delay High side or low side	$V_{LIN,HIN} = 0\text{V}$; $I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$	$t_{d(on)}$	-	639	-	ns
Turn-on rise time High side or low side	$V_{LIN,HIN} = 5\text{V}$; $I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$	t_r	-	34	-	
Turn-off propagation delay High side or low side	$V_{LIN,HIN} = 5\text{V}$; $I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$	$t_{d(off)}$	-	854	-	
Turn-off fall time High side or low side	$V_{LIN,HIN} = 0\text{V}$; $I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$	t_f	-	40	-	
Shutdown propagation delay ITRIP	$V_{ITRIP} = 1\text{V}$, I_u , I_v , $I_w = 10\text{A}$	t_{ITRIP}	-	1000	-	
Input filter time ITRIP	$V_{ITRIP} = 1\text{V}$	$t_{ITRIPmin}$	155	210	380	
Input filter time at LIN for turn on and off and input filter time at HIN for turn on only	$V_{LIN,HIN} = 0\text{V} \text{ \& } 5\text{V}$	t_{FILIN}	120	270	-	
Input filter time at HIN for turn off	$V_{HIN} = 5\text{V}$	t_{FILIN1}	-	220	-	
Input filter time at HIN for turn off	$V_{HIN} = 5\text{V}$	t_{FILIN2}	-	400	-	
Fault clear time after ITRIP-fault	$V_{LIN,HIN} = 0\text{V} \text{ \& } 5\text{V}$ $V_{ITRIP} = 0\text{V}$	t_{FLTCLR}	-	4.7	-	ms
Min. deadtime between low side and high side		DT_{PWM}	-	1.5	-	μs
Deadtime of gate drive circuit		DT_{IC}	-	380	-	ns
IGBT Turn-on Energy (includes reverse recovery of diode)	$I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	E_{on}	-	320	-	μJ
			-	430	-	
IGBT Turn-off Energy	$I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	E_{off}	-	200	-	
			-	270	-	
Diode recovery Energy	$I_{out} = 10\text{A}$, $V_{DC} = 300\text{V}$ $T_{vj} = 25^\circ\text{C}$ $T_{vj} = 150^\circ\text{C}$	E_{rec}	-	46	-	
			-	115	-	

Integrated Components

Description	Condition	Symbol ¹	Value			Unit
			min	typ	max	
Resistor		Rbs	-	10	-	Ω
Resistor	T _{NTC} = 25°C	RTS	-	100	-	kΩ
B-Constant of NTC (Negative Temperature Coefficient)	T _{NTC} = 25°C	B25	-	4250	-	K
Bootstrap diode forward voltage	I _{FDBS} = 100mA	V _{FDBS}	-	1.9	2.05	V
Capacitor		C1	-	100	-	nF
Capacitor		Cgex		0.39		
Bootstrap Capacitor		CbsH _x	-	100	-	

¹ Symbols according to Figure 1

Characteristics

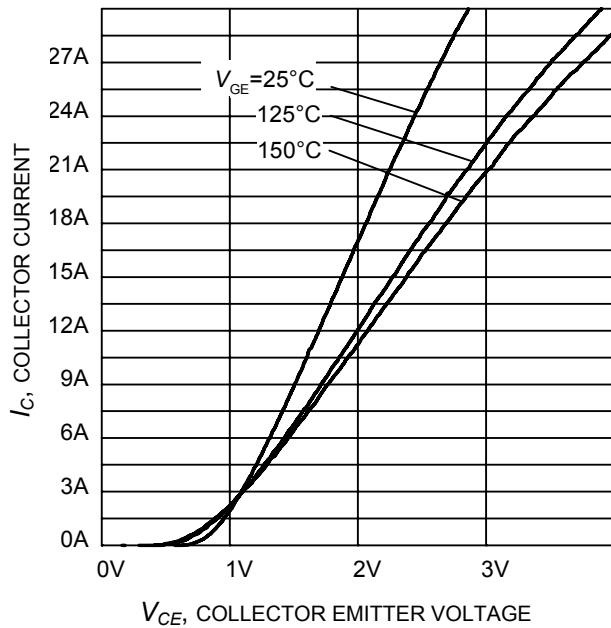


Figure 5. Typical IGBT output characteristic
($V_{DD} = 15V$)

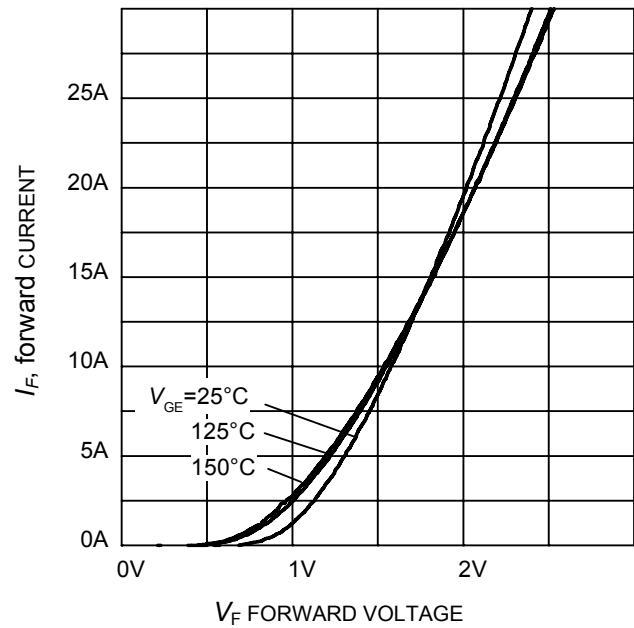


Figure 6. Typical diode forward current as a function of forward voltage

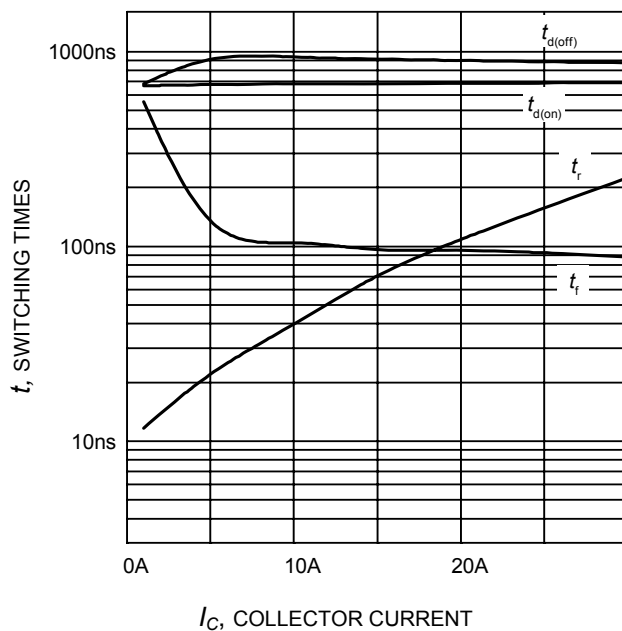


Figure 7. Typical switching times as a function of collector current
(inductive load, $T_J = 150^\circ C$,
 $V_{CE} = 300V$, $V_{DD} = 15V$
Dynamic test circuit in Figure A)

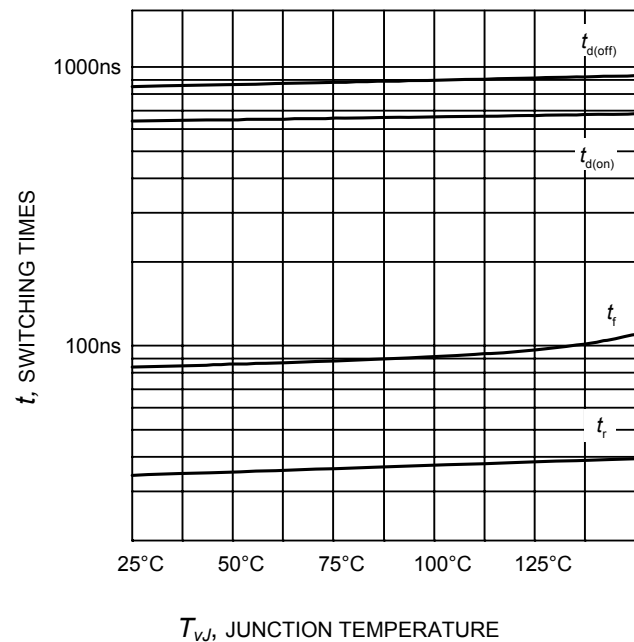


Figure 8. Typical switching times as a function of junction temperature
(inductive load, $V_{CE} = 300V$,
 $V_{DD} = 15V$, $I_C = 10A$
Dynamic test circuit in Figure A)

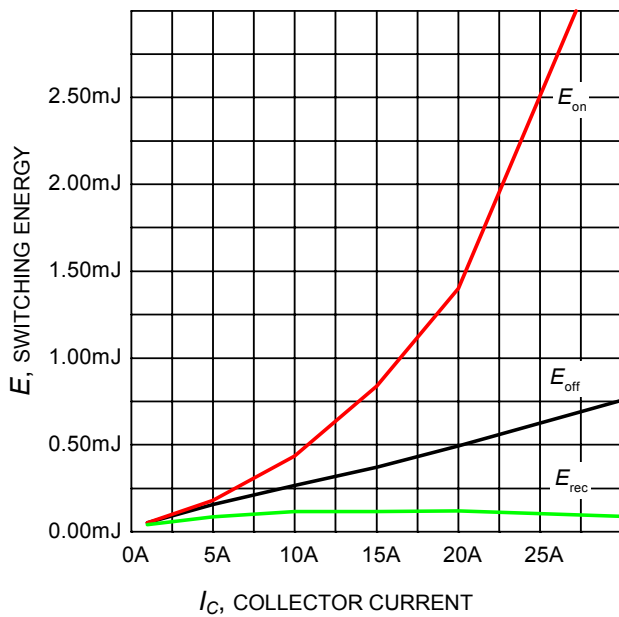


Figure 9. Typical switching energy losses as a function of collector current
(inductive load, $T_{vj} = 150^\circ\text{C}$,
 $V_{CE} = 300\text{V}$, $V_{DD} = 15\text{V}$
Dynamic test circuit in Figure A)

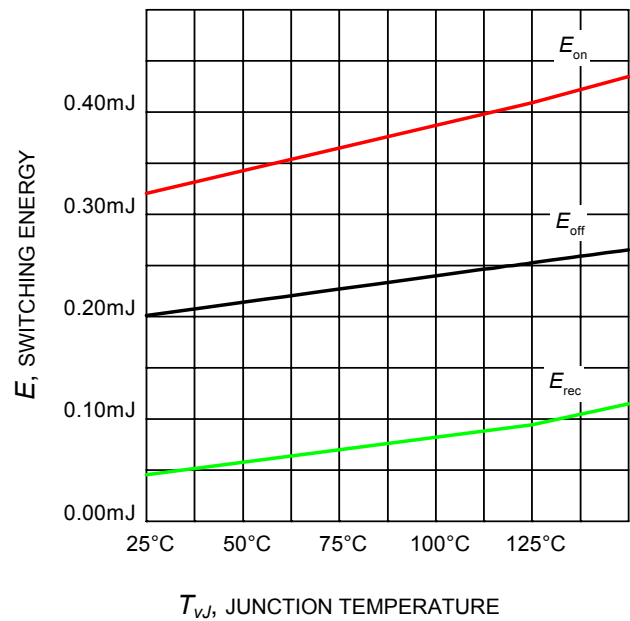


Figure 10. Typical switching energy losses as a function of junction temperature
(inductive load, $V_{CE} = 300\text{V}$,
 $V_{DD} = 15\text{V}$, $I_C = 10\text{A}$
Dynamic test circuit in Figure A)

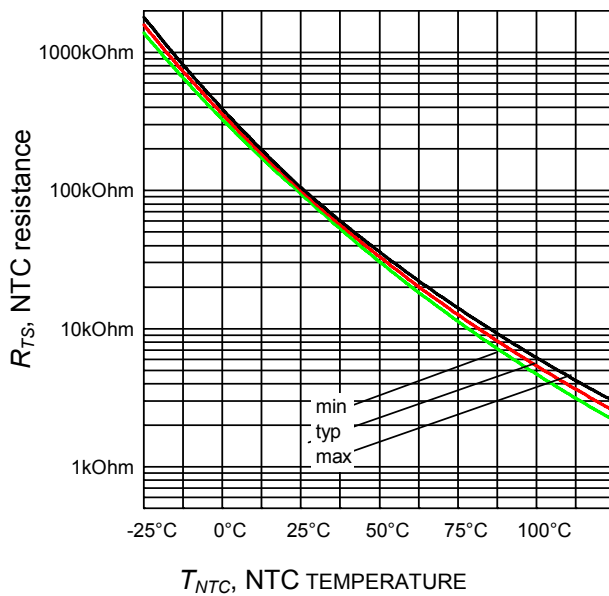


Figure 11. Characteristic of NTC as a function of NTC temperature

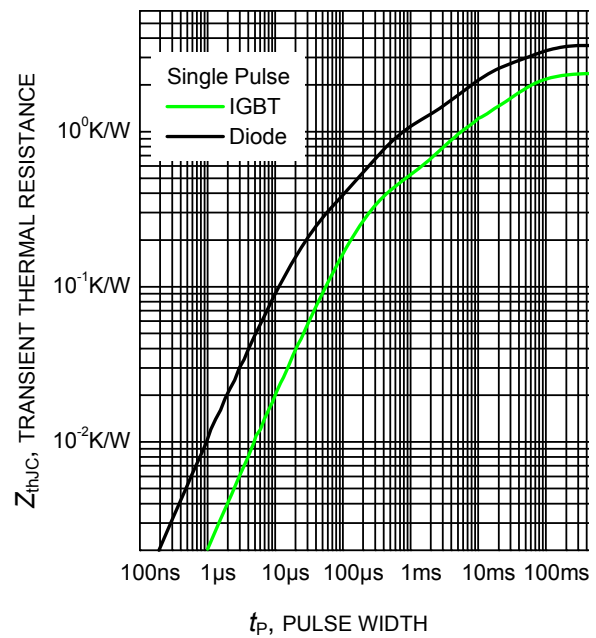


Figure 12. Transient thermal impedance as a function of pulse width
($D = t_p/T$)

Test Circuits and Parameter Definition

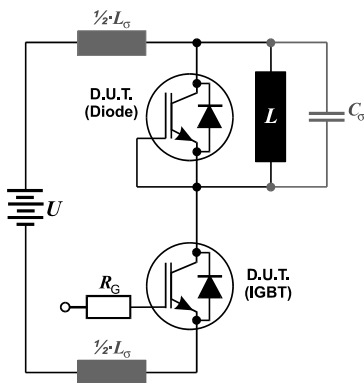


Figure A: Dynamic test circuit
Leakage inductance $L_{\sigma} = 180\text{nH}$
Stray capacitance $C_{\sigma} = 39\text{pF}$

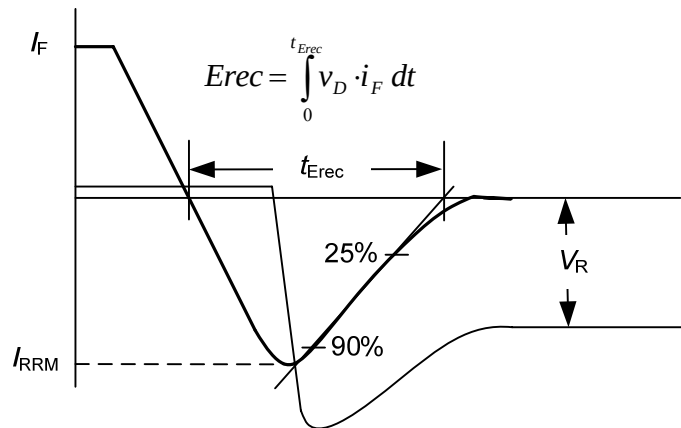


Figure B: Definition of diodes switching characteristics

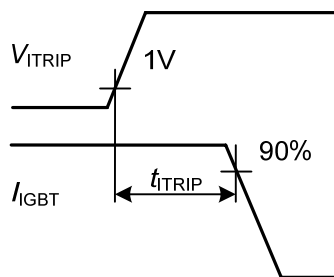


Figure C: Definition of ITIRP propagation delay

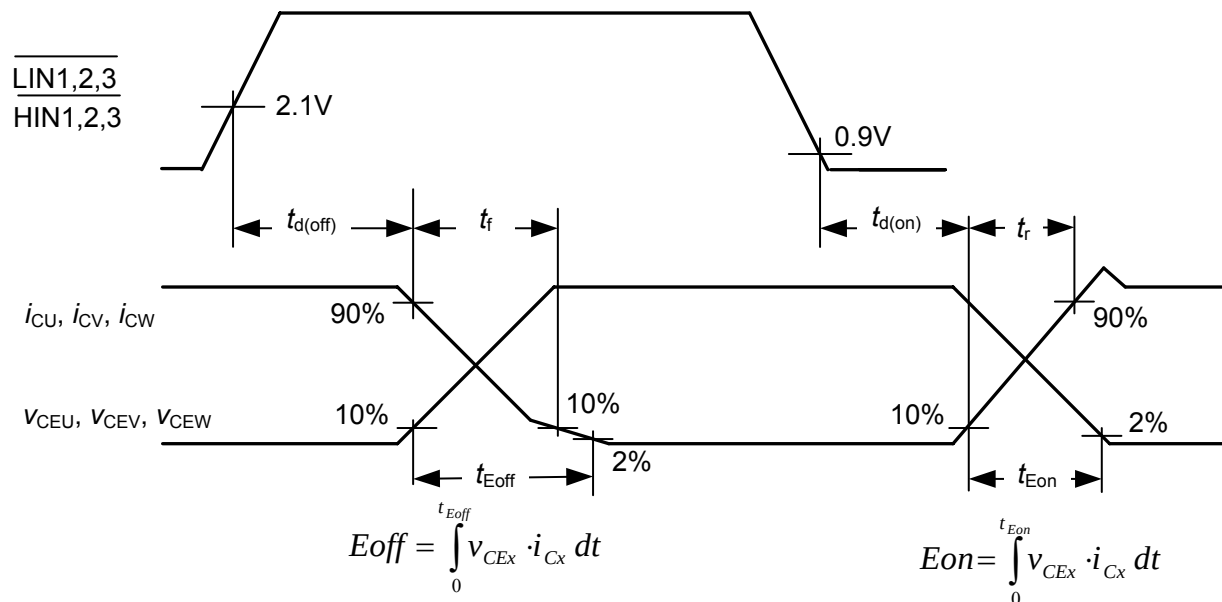


Figure D: Switching times definition and switching energy definition

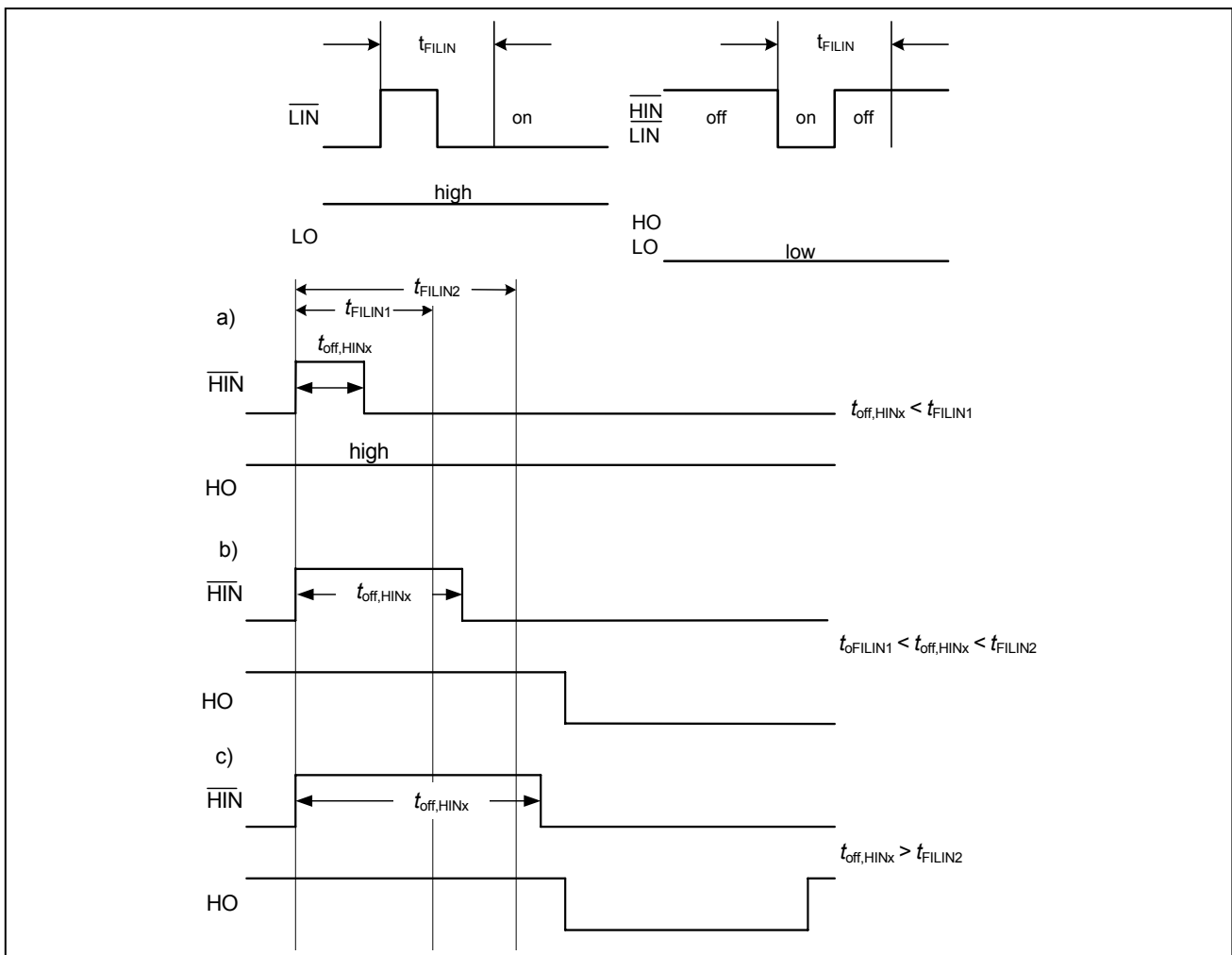


Figure E: Short Pulse suppression

Technical drawing of a 24-pin connector, showing three views: top, front, and side.

Top View:

- Overall width: 50.4 ± 0.3
- Overall height: 38 ± 0.3
- Pin pitch: $2.3 \times 2 = 4.6$
- Pin 1 location: Laser Marking - $\phi 1$
- Pin 1 tolerance: $\max. 0.12$ per side
- Pin 24 location: 0.8 ± 0.1
- Pin 2 location: 0.4 ± 0.1
- Pin 2 tolerance: 0.4 ± 0.1
- Pin 24 tolerance: 0.4 ± 0.1

Front View:

- Overall height: 31.95 ± 0.4
- Pin pitch: $2.3 \times 2 = 4.6$
- Pin 1 location: Laser Marking - $\phi 1$
- Pin 1 tolerance: $\max. 0.12$ per side
- Pin 24 location: 0.8 ± 0.1
- Pin 2 location: 0.4 ± 0.1
- Pin 2 tolerance: 0.4 ± 0.1
- Pin 24 tolerance: 0.4 ± 0.1

Side View:

- Overall height: 39.2
- Pin pitch: $2.3 \times 2 = 4.6$
- Pin 1 location: Laser Marking - $\phi 1$
- Pin 1 tolerance: $\max. 0.12$ per side
- Pin 24 location: 0.8 ± 0.1
- Pin 2 location: 0.4 ± 0.1
- Pin 2 tolerance: 0.4 ± 0.1
- Pin 24 tolerance: 0.4 ± 0.1

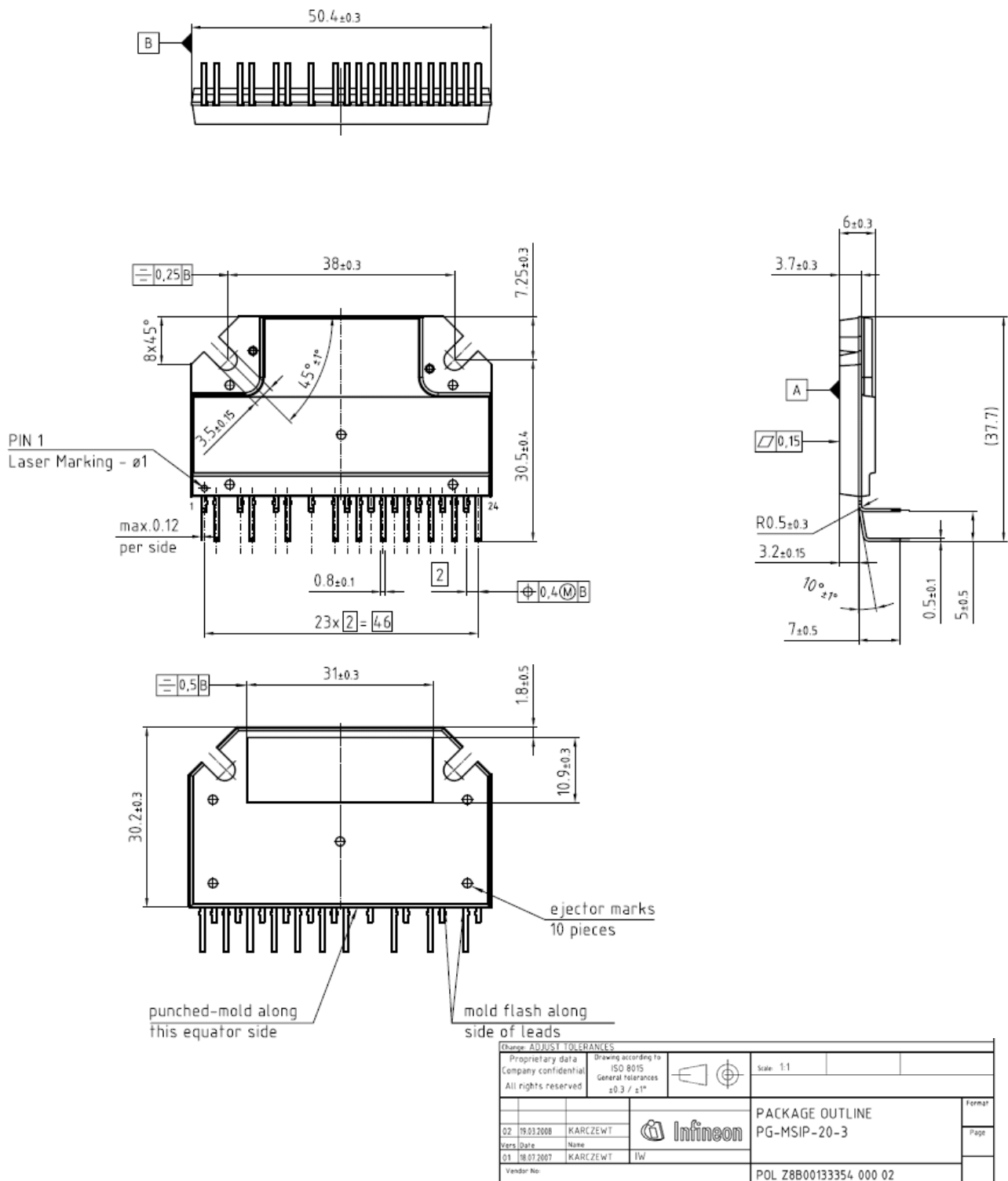
Other Features:

- Ejector marks: 10 pieces
- Mold flash along side of leads
- Punched-mold along this equator side

Proprietary data Company confidential All rights reserved		Drawing according to ISO 8015 General Tolerances ±0.3 / ±1°				Scale: 1:1			
04.	07.04.2008	KARCZEWT		 Infineon		PACKAGE OUTLINE PG-MSIP-20-1			Format A3
03.	19.07.2007	KARCZEWT							
02.	02.05.2007	KARCZEWT							
Vers. Date		Name							
01	09/05/2005	KOENIGSB	IW				Page 00		
Vendor No:				POL Z8B00002766 000 04					

Rev. 2.2, March 2009

Package Outline IKCS17F60B2C



Description	Condition	Symbol	Value			Unit
			min	typ	max	
Weight		m _P	-	17	-	g

Note: There may occur discolourations on the copper surface without any effect of the thermal properties.