

PM20CNJ060

FLAT-BASE TYPE
INSULATED PACKAGE

PM20CNJ060



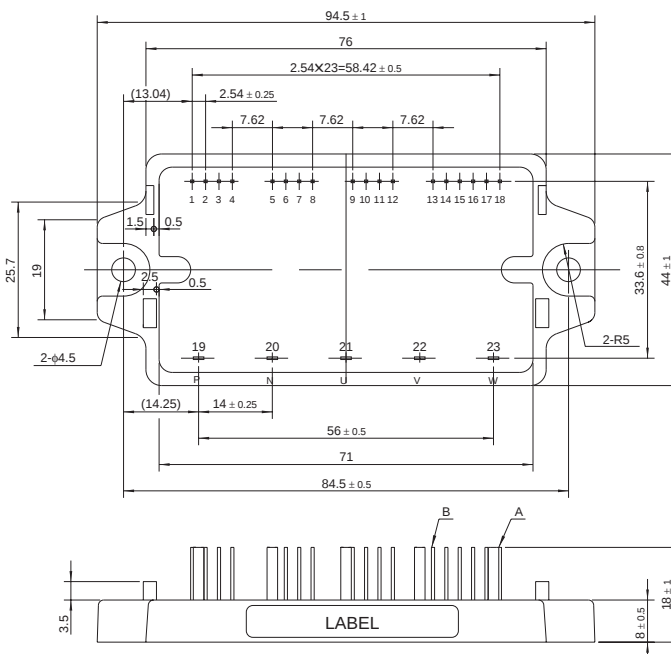
- 3 phase IGBT (20A/600V) inverter output
 - Monolithic gate drive & protection logic circuit
 - Protection logic
 - Over circuit (OC)
 - Short circuit (SC)
 - Over temperature (OT)
 - Under voltage lock-out (UV)
 - UL Recognized
- File No. E80271
Yellow Card No. E80276

APPLICATION

General purpose inverter, servo drives and other motor controllers

PACKAGE OUTLINES

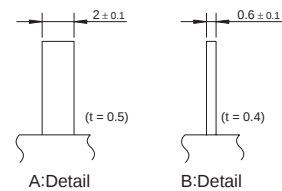
Dimensions in mm



Terminal code

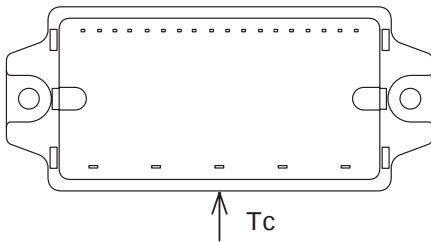
1. VUPC	13. VNC
2. NC	14. VN1
3. UP	15. UN
4. VUP1	16. VN
5. VVPC	17. WN
6. NC	18. FO
7. VP	19. P
8. VVP1	20. N
9. VWPC	21. U
10. NC	22. V
11. WP	23. W
12. VWP1	

NC : No Connect



PM20CNJ060**FLAT-BASE TYPE
INSULATED PACKAGE****TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Supply Voltage Protected by SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _J = 125°C Start	400	V
V _{CC(surge)}	Supply Voltage	Applied between : P-N, Surge value	500	V
T _C	Module Case Operating Temperature	(Note-1)	-20 ~ +100	°C
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	V _{rms}

(Note-1) T_C measurement point**ELECTRICAL CHARACTERISTICS** (T_J = 25°C, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 20A V _{CIN} = 0V, Pulsed (Fig. 1)	T _J = 25°C T _J = 125°C	—	1.8 1.9	2.5 2.6	V
V _{EC}	FWDi Forward Voltage	-I _C = 20A, V _D = 15V, V _{CIN} = 15V (Fig. 2)		—	2.5	3.5	V
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 0V↔15V V _{CC} = 300V, I _C = 20A T _J = 125°C, Inductive Load (Upper-Lower Arm) (Fig. 3)		0.3	0.7	1.6	μs
t _{rr}				—	0.15	0.5	μs
t _{c(on)}				—	0.4	1.1	μs
t _{off}				—	1.5	2.3	μs
t _{c(off)}				—	0.5	1.5	μs
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _D = 15V (Fig. 4)	T _J = 25°C T _J = 125°C	—	—	1 10	mA

PM20CNJ060**FLAT-BASE TYPE
INSULATED PACKAGE****CONTROL PART**

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
ID	Circuit Current	VD = 15V, V _{CIN} = 15V	VN1-VNC	—	18	25	mA
			VXP1-VXPC	—	7	10	
V _{th(ON)}	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC		1.2	1.5	1.8	V
V _{th(OFF)}	Input OFF Voltage			1.7	2.0	2.3	V
OC	Over Current Trip Level	−20 ≤ TJ ≤ 125°C, VD = 15V (Fig. 5,6)		28	38	—	A
SC	Short Circuit Trip Level	−20 ≤ TJ ≤ 125°C, VD = 15V (Fig. 5,6)		—	57	—	A
toff(OC)	Over Current Delay Time	VD = 15V (Fig. 5,6)		—	10	—	μs
OT	Over Temperature protection	VD = 15V	Trip level	100	110	120	°C
OT _r			Reset level	—	90	—	°C
UV	Supply Circuit Under-Voltage Protection	−20 ≤ TJ ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV _r			Reset level	—	12.5	—	V
I _{FO(H)}	Fault Output Current	VD = 15V, V _{CIN} = 15V (Note-2)	—	—	0.01	mA	
I _{FO(L)}			—	10	15	mA	
t _{FO}	Minimum Fault Output Pulse Width	VD = 15V (Note-2)		1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

THERMAL RESISTANCES

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal	Inverter IGBT part (per 1/6 module)	—	—	2.2	°C/W
R _{th(j-c)F}	Resistances	Inverter FWDi part (per 1/6 module)	—	—	4.5	°C/W
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	—	—	0.5	°C/W

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M4	0.98	1.18	1.47	N • m
—	Weight	—	10	12	15	kg • cm
—	Weight	—	—	60	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals (Fig. 3)	≤ 400	V
V _D	Control Supply Voltage	Applied between : V _{UP1} -V _{UPC} , V _{VP1} -V _{VPC} V _{WP1} -V _{WPC} , V _{N1} -V _{Nc} (Note-3)	15 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-V _{UPC} , VP-V _{VPC} , WP-V _{WPC} U _N • V _N • W _N -V _{Nc}	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 4.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 15	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2	μs

(Note-3) With ripple satisfying the following conditions
dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

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PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input signals should be low level.
After this, each input signal should be set to the specified ON and OFF level.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above $V_{CC(surge)}$ rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

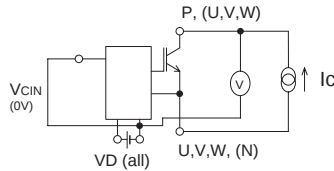


Fig. 1 $V_{CE(sat)}$ Test

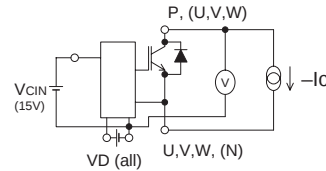
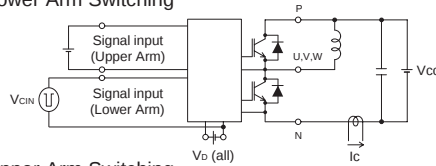


Fig. 2 V_{EC} Test

a) Lower Arm Switching



b) Upper Arm Switching

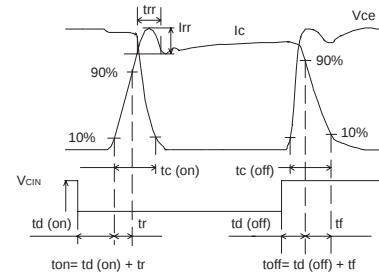
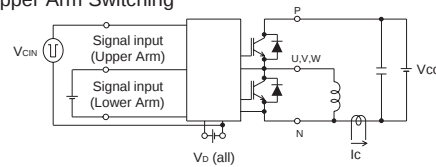


Fig. 3 Switching time Test circuit and waveform

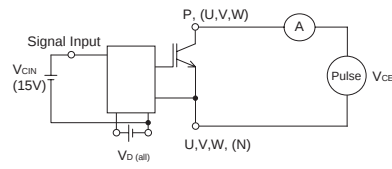


Fig. 4 I_{CES} Test

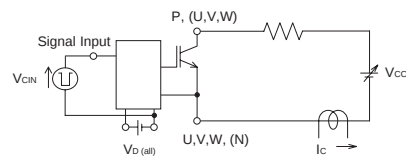
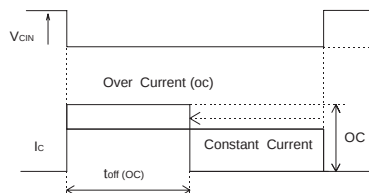


Fig. 5 OC and SC Test

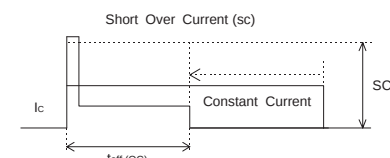


Fig. 6 OC and SC Test waveform

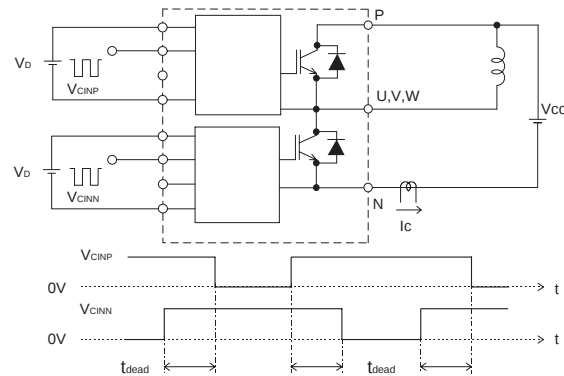


Fig. 7 Dead time measurement point example

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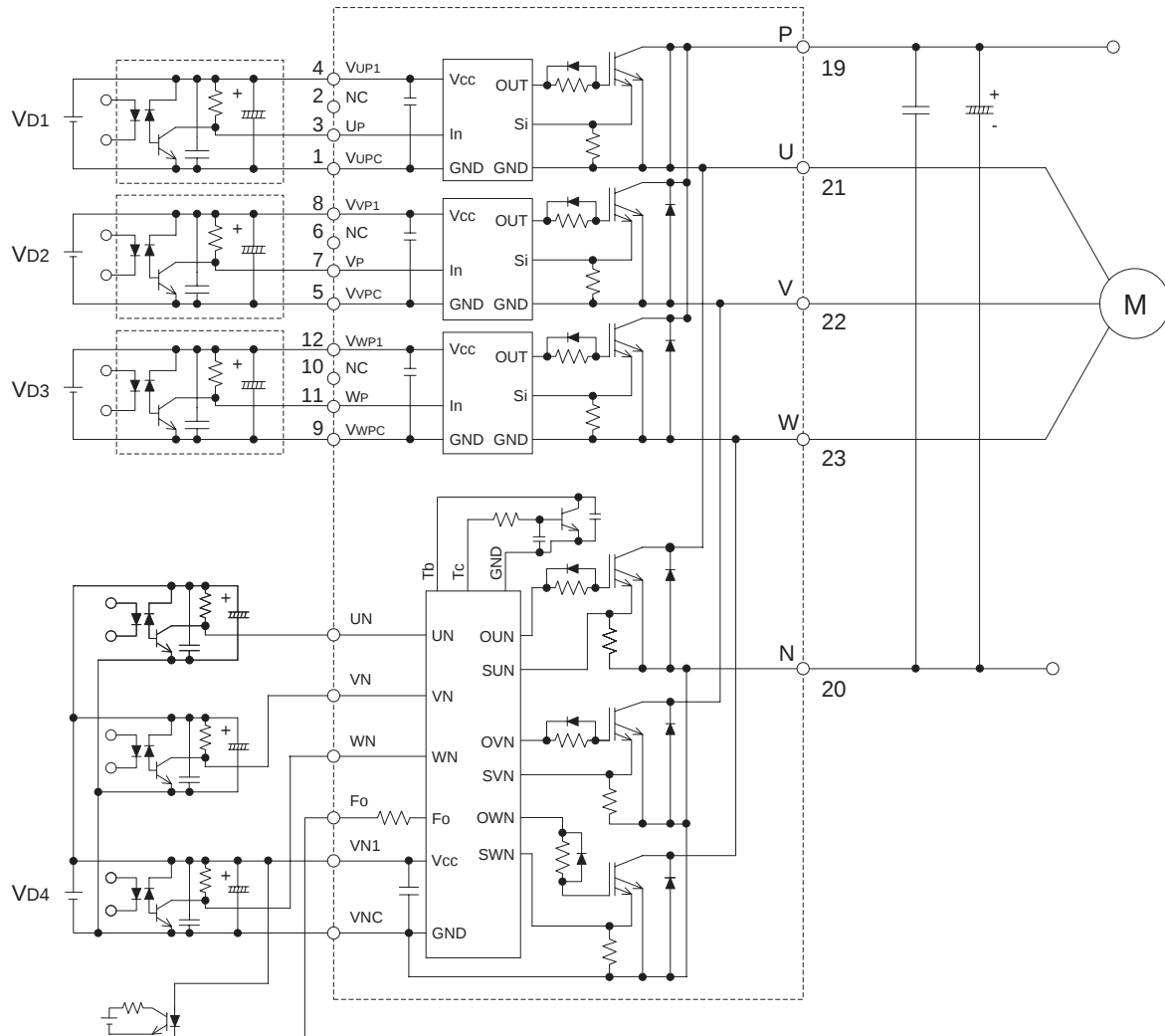


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.