

TERMINAL CODE		
1	VUFS	20 VNO
2	(UPG)	21 UN
3	VUFB	22 VN
4	VP1	23 WN
5	(COM)	24 FO
6	UP	25 CFO
7	VVFS	26 CIN
8	(VPG)	27 VNC
9	VVFB	28 VN1
10	VP1	29 (WNG)
11	(COM)	30 (VNG)
12	VP	31 NW
13	VWFS	32 NV
14	(WPG)	33 NU
15	VWFB	34 UW
16	VP1	35 V
17	(COM)	36 U
18	WP	37 P
19	(UNG)	38 NC

PS21767-V

TRANSFER-MOLD TYPE
INSULATED TYPE

MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-NU, NV, NW	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
V _{CES}	Collector-emitter voltage		600	V
±I _C	Each IGBT collector current	$T_c = 25^\circ\text{C}$	30	A
±I _{CP}	Each IGBT collector current (peak)	$T_c = 25^\circ\text{C}$, less than 1ms	60	A
P _C	Collector dissipation	$T_c = 25^\circ\text{C}$, per 1 chip	90.9	W
T _j	Junction temperature		-20~+150	°C

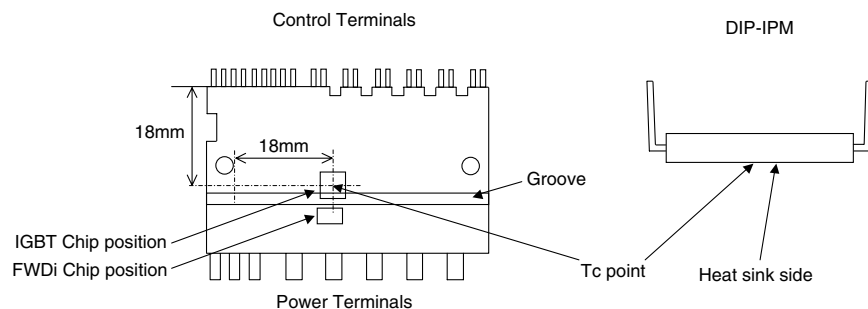
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(PROT)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T _c	Module case operation temperature	(Note 1)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, All pins to heat-sink plate	2500	V _{rms}

Note 1 : T_c measurement point



PS21767-V

TRANSFER-MOLD TYPE

INSULATED TYPE

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 2)	Inverter IGBT part (per 1/6 module)	—	—	1.1	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	—	—	2.8	°C/W

Note 2 : Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

The contacting thermal resistance between DIP-IPM case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/m·k

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}$	—	1.70	2.20	V
V_{EC}	FWDi forward voltage	$T_j = 25^\circ\text{C}$, $-I_C = 30\text{A}$, $V_{IN} = 0\text{V}$	—	1.50	2.00	V
t_{on}	Switching times	$V_{CC} = 300\text{V}$, $V_D = V_{DB} = 15\text{V}$ $I_C = 30\text{A}$, $T_j = 125^\circ\text{C}$, $V_{IN} = 0 \leftrightarrow 5\text{V}$ Inductive load (upper-lower arm)	0.70	1.30	1.90	μs
t_{rr}			—	0.30	—	μs
$t_{c(on)}$			—	0.50	0.80	μs
t_{off}			—	1.50	2.10	μs
$t_{c(off)}$			—	0.35	0.55	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$ $T_j = 25^\circ\text{C}$	—	—	1	mA
		$T_j = 125^\circ\text{C}$	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
Id	Circuit current	VD = VDB = 15V VIN = 5V	Total of VP1-VNC, VN1-VNC	—	—	7.00	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	0.55	mA
		VD = VDB = 15V VIN = 0V	Total of VP1-VNC, VN1-VNC	—	—	7.00	mA
			VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	—	—	0.55	mA
VFOH	Fault output voltage	VSC = 0V, Fo terminal pull-up to 5V with 10kΩ		4.9	—	—	V
VFOL		VSC = 1V, IFO = 1mA		—	—	0.95	V
VSC(ref)	Short circuit trip level	Tj = 25°C, VD = 15V (Note 3)		0.43	0.48	0.53	V
IIN	Input current	VIN = 5V		1.0	1.5	2.0	mA
UVDBt	Control supply under-voltage protection	Tj ≤ 125°C	Trip level	10.0	—	12.0	V
UVDBr			Reset level	10.5	—	12.5	V
UVDt			Trip level	10.3	—	12.5	V
UVDr			Reset level	10.8	—	13.0	V
tFO	Fault output pulse width	CFO = 22nF (Note 4)		1.0	1.8	—	ms
Vth(on)	ON threshold voltage	Applied between UP, VP, WP, UN, VN, WN-VNC		—	2.3	2.6	V
Vth(off)	OFF threshold voltage			0.8	1.4	—	V
Vth(hys)	ON/OFF threshold hysteresis voltage			0.5	0.9	—	V

Note 3 : Short circuit protection is functioning only at the low-arms. Please select the external shunt resistance such that the SC trip-level is less than 2.0 times of the current rating.

4 : Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions works. The fault output pulse-width t_{FO} depends on the capacitance of C_{FO} according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO} [\text{F}]$.

PS21767-V

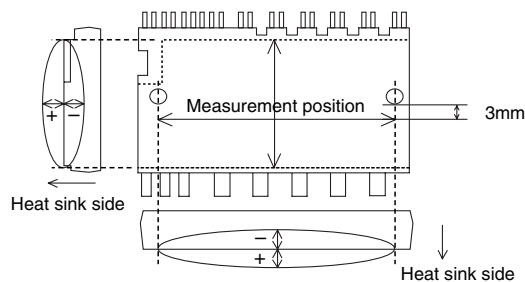
TRANSFER-MOLD TYPE

INSULATED TYPE

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	Recommended : 0.78 N·m	0.59	—	0.98	N·m
Weight			—	21	—	g
Heat-sink flatness	(Note 5)		-50	—	100	μm

Note 5 : Flatness measurement position



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Recommended value			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V _D	Control supply voltage	Applied between VP1-VNC, VN1-VNC	13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.0	15.0	18.5	V
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs
t _{dead}	Arm shoot-through blocking time	For each input signal, T _c ≤ 100°C	2	—	—	μs
f _{PWM}	PWM input frequency	T _c ≤ 100°C, T _j ≤ 125°C	—	—	20	kHz
I _O	Output r.m.s. current	V _{CC} = 300V, V _D = V _{DB} = 15V, P.F = 0.8, sinusoidal PWM T _c ≤ 100°C, T _j ≤ 125°C (Note 6)	f _{PWM} = 5kHz —	—	21	Arms
			f _{PWM} = 15kHz —	—	16	
P _{WIN(on)}	Minimum input pulse width	(Note 7)	0.3	—	—	μs
		200 ≤ V _{CC} ≤ 350V, 13.5 ≤ V _D ≤ 16.5V, 13.0 ≤ V _{DB} ≤ 18.5V, -20°C ≤ T _c ≤ 100°C, N-line wiring inductance less than 10nH (Note 8)	Below rated current 1.6	—	—	
			Between rated current and 1.7 times of rated current 3.3	—	—	
			Between 1.7 times and 2.0 times of rated current 3.9	—	—	
V _N	V _N voltage variation	Between V _N -NU, NV, NW (including surge)	-5.0	—	5.0	V
T _j	Junction temperature		-20	—	125	°C

Note 6 : The allowable r.m.s. current value depends on the actual application conditions.

7 : Input signal with ON pulse width less than P_{WIN(on)} might make no response.

8 : IPM might make delayed response (less than about 2μsec) or no response for the input signal with off pulse width less than P_{WIN(off)}. Please refer Fig. 2 about delayed response and Fig. 6 about N-line inductance.

PS21767-V

TRANSFER-MOLD TYPE
INSULATED TYPE

Fig. 2 ABOUT DELAYED RESPONSE AGAINST SHORTER INPUT OFF SIGNAL THAN PWIN (off) (P side only)

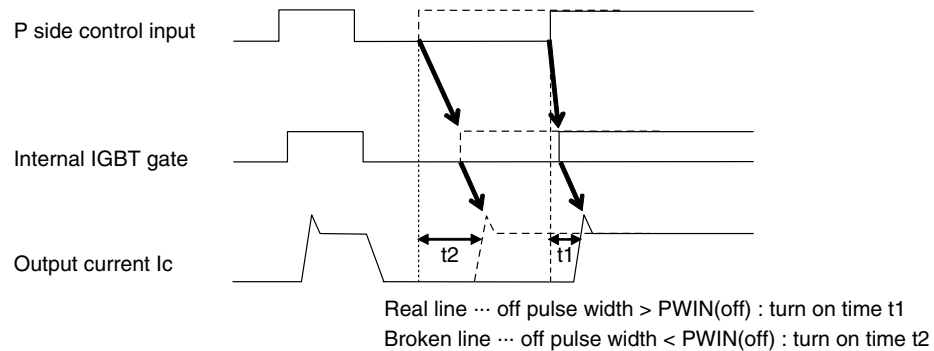


Fig. 3 THE DIP-IPM INTERNAL CIRCUIT

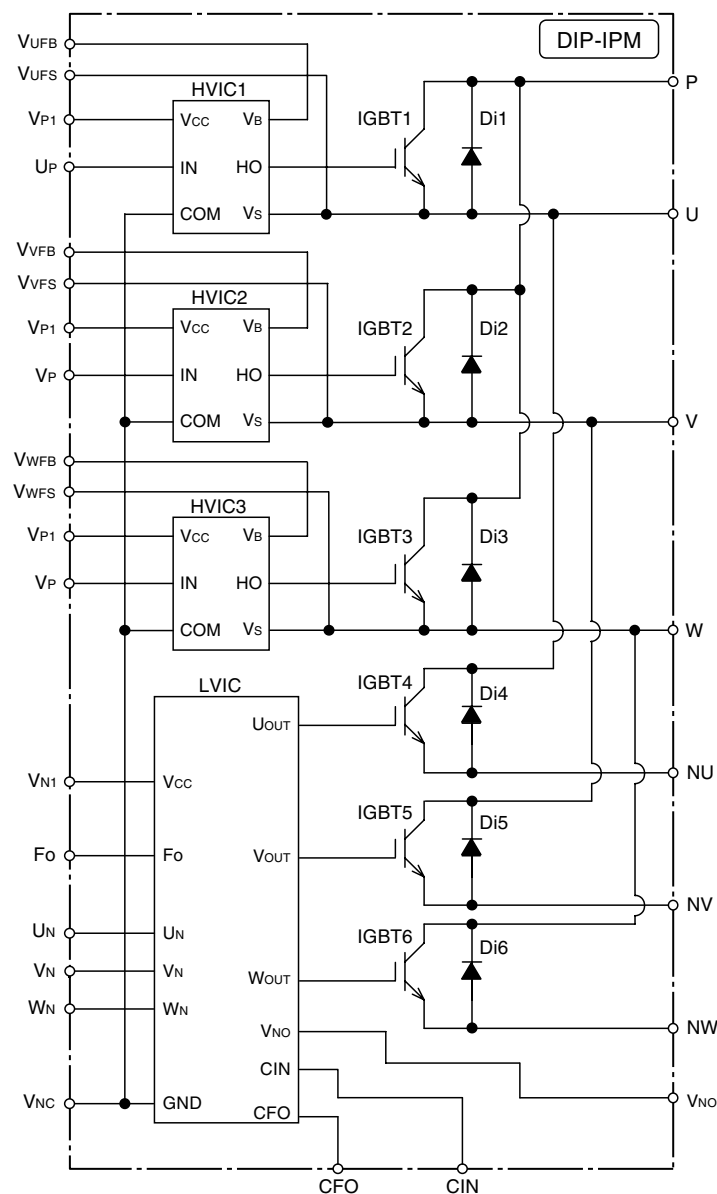
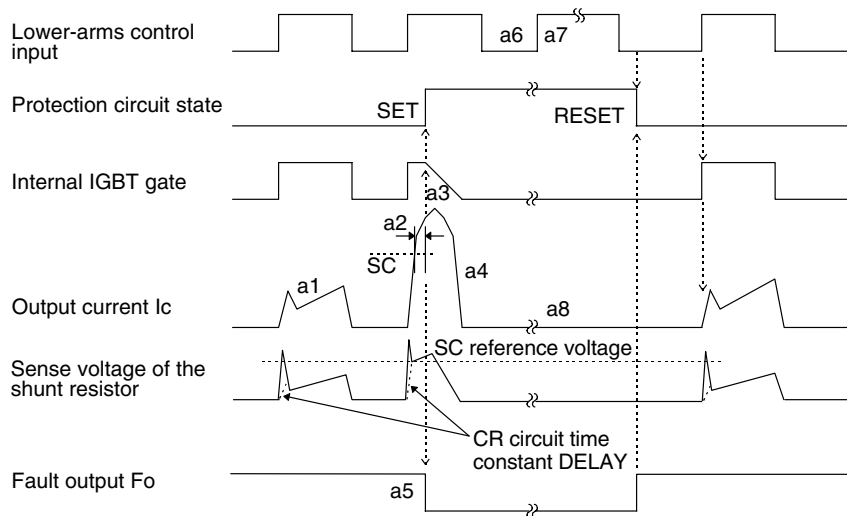


Fig. 4 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

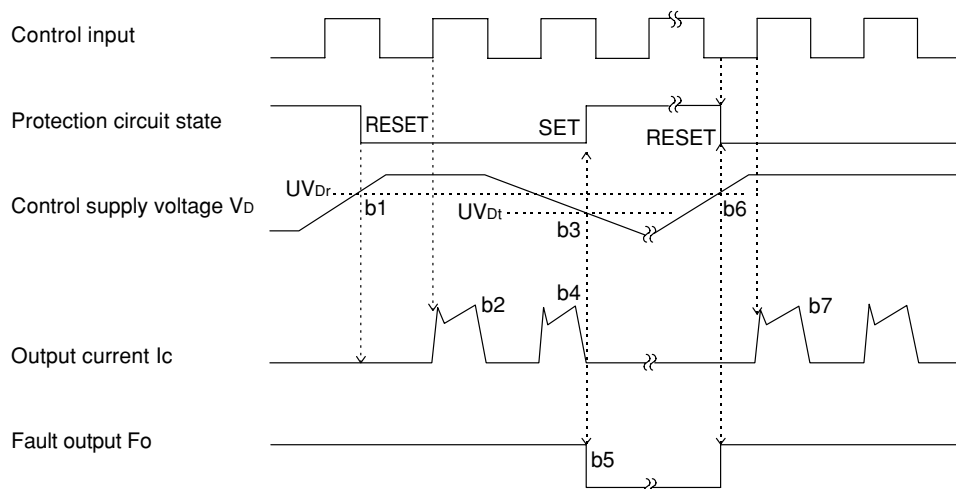
[A] Short-Circuit Protection (Lower-arms only with the external shunt resistor and CR filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a6. Input "L" : IGBT OFF.
- a7. Input "H"
- a8. IGBT OFF state in spite of input "H".



[B] Under-Voltage Protection (Lower-arm, UV_D)

- b1. Control supply voltage rising : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT turns OFF in spite of control input condition.
- b5. Fo operation starts.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (Upper-arm, UVDB)

- c1. Control supply voltage rises : After the voltage level reaches UVDBr, the circuits start to operate.
- c2. Protection circuit state reset : IGBT ON and carrying current.
- c3. Normal operation : IGBT ON and carrying current.
- c4. Under-voltage trip (UVDBt).
- c5. IGBT OFF inspite of control input condition, but there is no Fo signal output.
- c6. Under-voltage reset (UVDBr).
- c7. Normal operation : IGBT ON and carrying current.

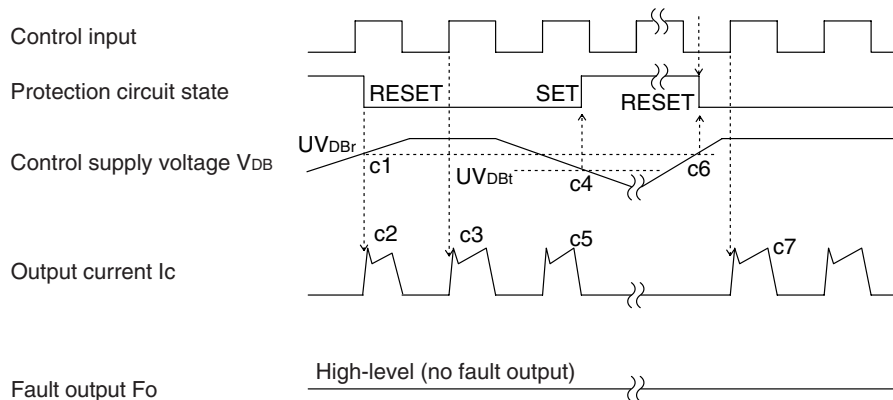
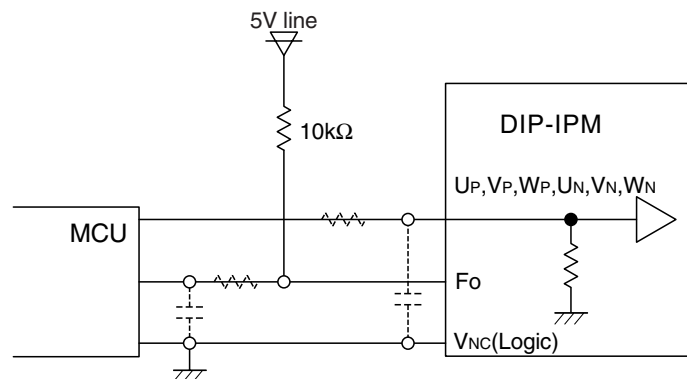
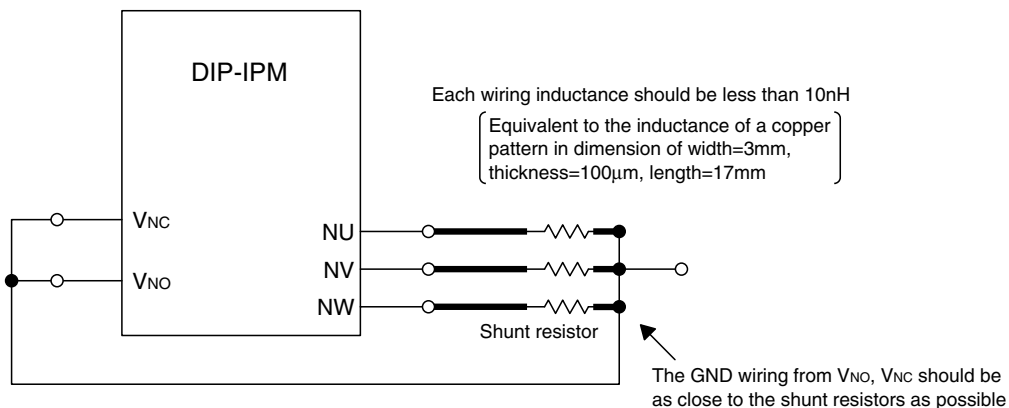


Fig. 5 RECOMMENDED MCU I/O INTERFACE CIRCUIT



Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board.
The DIP-IPM input signal section integrates a 2.5kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

Fig. 6 RECOMMENDED WIRING AROUND THE SHUNT RESISTOR



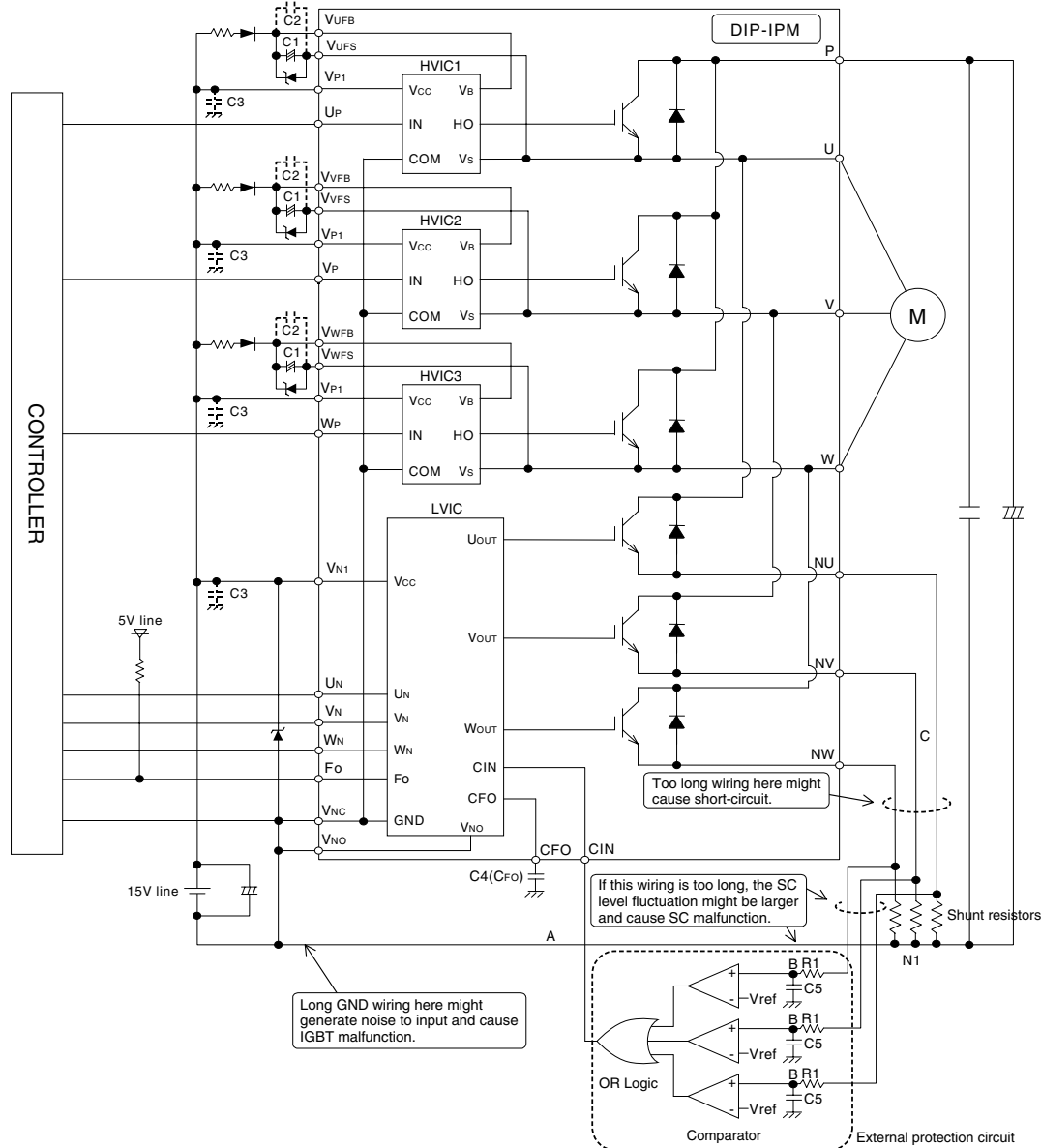
PS21767-V

TRANSFER-MOLD TYPE

INSULATED TYPE

Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE

C1: Tight tolerance temp-compensated electrolytic type C2,C3: 0.22~2μF R-category ceramic capacitor for noise filtering



- Note 1** : Input drive is High-active type. There is a 2.5kΩ(Min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
- 2** : Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
- 3** : Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.
Fo output pulse width is determined by the external capacitor (CFO) between CFO and VNC terminals (e.g CFO = 22nF → tFO = 1.8ms (typ.))
- 4** : To prevent erroneous protection, the wiring of A, B should be as short as possible.
- 5** : The time constant R1C5 of the protection circuit should be selected in the range of 1.5~2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C5.
- 6** : All capacitors should be mounted as close to the terminals of the DIP-IPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3: good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- 7** : To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1~0.22μF snubber between the P-N1 terminals is recommended.
- 8** : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 9** : If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.
- 10** : The reference voltage Vref of comparator should be set up the same rating of short circuit trip level (Vsc(ref): min.0.43V to max.0.53V).
- 11** : OR logic output high level should exceed the maximum short circuit trip level (Vsc(ref): max.0.53V).